WHAT IS CLAIMED IS:

1. A method for operating a memory system, the memory system including a non-volatile memory, the non-volatile memory having a plurality of physical blocks and a plurality of data structures including an erase count block, the erase count block containing a status of each physical block of the plurality of physical blocks, the method comprising:

determining when contents of at least one data structure of the plurality of data structures are to be updated;

queuing a request to update the contents of the at least one data structure when it is determined that the contents of the at least one data structure are to be updated; and

executing the request to update the contents of the at least one data structure.

2. The method of claim 1 updating the contents of the at least one data structure includes updating the contents of the erase count block to indicate a substantially current status of each physical block of the plurality of physical blocks.

3. The method of claim 1 wherein the plurality of data structures includes a first data structure arranged to contain information which identifies available physical blocks of the plurality of physical blocks which have been through a relatively low number of write and erase cycles as indicated by the status associated with the available physical blocks, and wherein executing the request to update the contents of the at least one data structure includes updating contents of the first data structure.

4. The method of claim 1 wherein the plurality of data structures includes a first data structure arranged to contain information which identifies available physical blocks of the plurality of physical blocks which have been through a relatively high number of write and erase cycles as indicated by the status associated with the available physical blocks, and wherein executing the request to update the contents of the at least one data structure includes updating contents of the first data structure.

5. The method of claim 1 wherein the plurality of data structures includes a first data structure that is arranged to contain information which is used by the memory system when the memory system is powered up, and wherein executing the request to update the contents of the at least one data structure includes updating contents of the first data structure.

6. The method of claim 5 wherein the first data structure is a power management block.

7. The method of claim 1 wherein queuing the request to update the contents of the at least one data structure includes:

adding the request to a queue of procedures and applications to be executed, the request being assigned a relatively low priority in the queue.

8. The method of claim 7 wherein executing the request to update the contents of the at least one data structure includes executing the request to update the contents of the at least one data structure when the queue is substantially empty except for the request to update the contents of the at least one data structure.

9. The method of claim 1 wherein determining when the contents of the at least one data structure of the plurality of data structures are to be updated includes comparing a first value with a threshold, wherein when the first value is substantially equal to the threshold, it is determined that the contents of the at least one data structure are to be updated.

10. The method of claim 1 wherein determining when the contents of the at least one data structure of the plurality of data structures are to be updated includes obtaining a time associated with the memory system and determining when the time indicates that the contents of the at least one data structure are to be updated.

11. The method of claim 1 wherein the non-volatile memory is a NAND flash memory.

12. A method for operating a memory system, the memory system including a non-volatile memory, the non-volatile memory having a plurality of physical blocks and a plurality of data structures including an erase count block, the erase count block containing an erase count of at least one physical block of the plurality of physical blocks, the erase count being arranged to indicate a number of times the at least one physical block of the plurality of physical blocks has been erased, the method comprising:

determining when an internal maintenance process is to be performed within the memory system, wherein the internal maintenance process is arranged to update the erase count of the at least one physical block of the plurality of physical blocks in the erase count block;

queuing a request for the internal maintenance process when it is determined that the internal maintenance request is to be performed; and

executing the internal maintenance process.

13. The method of claim 12 wherein executing the internal maintenance process includes:

updating the erase count of the at least one physical block in the plurality of physical blocks in the erase count block; and

updating a first data structure of the plurality of data structures, the first data structure being arranged to contain information used when the memory system is powered up, wherein the information includes the erase count of the at least one physical block in the plurality of physical blocks.

14. The method of claim 13 wherein executing the internal maintenance process further includes:

updating contents of a second data structure of the plurality of data structures, the second data structure being arranged to substantially identify a set of physical blocks in the plurality of physical blocks which have relatively low erase counts; and

updating contents of a third data structure of the plurality of data structures, the third data structure being arranged to substantially identify a set of physical blocks in the plurality of physical blocks which have relatively high erase counts.

15. The method of claim 12 wherein determining when the internal maintenance process is to be performed includes comparing a first value with a threshold, wherein when the first value is substantially equal to the threshold, it is determined that the internal maintenance process is to be performed.

16. The method of claim 12 wherein determining when the internal maintenance process is to be performed includes obtaining a time associated with the memory system and determining when the time indicates that the internal maintenance process is to be performed.

17. A memory device comprising:

a non-volatile memory, the non-volatile memory including a plurality of physical blocks and an erase count block that is arranged to store an erase count associated with at least one physical block of the plurality of physical blocks;

code devices that are arranged to determine when an internal maintenance process is to be performed within the memory system, wherein the internal maintenance process is arranged to update the erase count of the at least one physical block of the plurality of physical blocks in the erase count block;

code devices that are arranged to queue a request for the internal maintenance process when it is determined that the internal maintenance request is to be performed;

code devices that are arranged to execute the internal maintenance process; and

a medium that stores the code devices.

18. The memory device of claim 17 wherein the code devices that are arranged to execute the internal maintenance process include:

code devices that are arranged to update the erase count of the at least one physical block in the plurality of physical blocks in the erase count block; and

code devices that are arranged to update a first data structure of the plurality of data structures, the first data structure being arranged to contain information used when the memory system is powered up, wherein the information includes the erase count of the at least one physical block in the plurality of physical blocks.

19. The memory device of claim 18 wherein the code devices that are arranged to execute the internal maintenance process further include:

code devices that are arranged to update contents of a second data structure of the plurality of data structures, the second data structure being arranged to substantially identify a set of physical blocks in the plurality of physical blocks which have relatively low erase counts; and

code devices that are arranged to update contents of a third data structure of the plurality of data structures, the third data structure being arranged to substantially identify a set of physical blocks in the plurality of physical blocks which have relatively high erase counts.

20. The memory device of claim 17 wherein the code devices that are arranged to determine when the internal maintenance process is to be performed include code devices that are arranged to compare a first value with a threshold, wherein when the first value is substantially equal to the threshold, it is determined that the internal maintenance process is to be performed.

21. The memory device of claim 17 wherein the code devices that are arranged to determine when the internal maintenance process is to be performed include code devices that are arranged to obtain a time associated with the memory system and code devices

that are arranged to determine when the time indicates that the internal maintenance process is to be performed.

22. A memory device comprising:

a non-volatile memory, the non-volatile memory including a plurality of physical blocks and an erase count block that is arranged to store an erase count associated with at least one physical block of the plurality of physical blocks;

means for determining when an internal maintenance process is to be performed within the memory system, wherein the internal maintenance process is arranged to update the erase count of the at least one physical block of the plurality of physical blocks in the erase count block;

means for queuing a request for the internal maintenance process when it is determined that the internal maintenance request is to be performed; and

means for executing the internal maintenance process.

23. The memory device of claim 22 wherein the means for executing the internal maintenance process include:

means for updating the erase count of the at least one physical block in the plurality of physical blocks in the erase count block; and

means for updating a first data structure of the plurality of data structures, the first data structure being arranged to contain information used when the memory system is powered up, wherein the information includes the erase count of the at least one physical block in the plurality of physical blocks.

24. The memory device of claim 23 wherein the means for executing the internal maintenance process further include:

means for updating contents of a second data structure of the plurality of data structures, the second data structure being arranged to substantially identify a set of physical blocks in the plurality of physical blocks which have relatively low erase counts; and

means for updating contents of a third data structure of the plurality of data structures, the third data structure being arranged to substantially identify a set of physical blocks in the plurality of physical blocks which have relatively high erase counts.

25. The memory device of claim 22 wherein the means for determining when the internal maintenance process is to be performed include means for comparing a first value with a threshold, wherein when the first value is substantially equal to the threshold, it is determined that the internal maintenance process is to be performed.

26. The memory device of claim 22 wherein the means for determining when the internal maintenance process is to be performed include means for obtaining a time associated with the memory system and means for determining when the time indicates that the internal maintenance process is to be performed.